Claims

1. A non-volatile memory cell, comprising:

a ferroelectric capacitor for selectively storing one of a plurality of polarization states,

means for applying a voltage pulse to said ferroelectric capacitor to generate a charge signal therefrom for reading the polarization state of said ferroelectric capacitor,

means for receiving said charge signal from said ferroelectric capacitor, and

means for connecting said ferroelectric capacitor to said means for receiving to transfer said charge signal therebetween upon receipt of a selection signal for said memory cell by said means for connecting.

2. A non-volatile memory cell as recited in claim 1 wherein said means for applying a voltage pulse comprises a drive line decoder for generating said voltage pulse and a drive line for transferring said pulse from said decoder to said ferroelectric capacitor.

3. A non-volatile memory cell as recited in claim 1 wherein said means for receiving said charge signal is a bit line connected to a sense amplifier which detects the charge signal on said bit line.

4. A non-volatile memory cell as recited in claim 1 wherein said means for connecting said ferroelectric capacitor comprises an MOS transistor having the gate terminal connected to receive said selection signal and the source and drain terminals connected between said ferroelectric capacitor and said means for receiving said charge signal.

5. A non-volatile memory cell as recited in claim 1 wherein said ferroelectric capacitor is connected between said means for applying a voltage pulse and said means for connecting.

6. A non-volatile memory cell as recited in claim 1 wherein said ferroelectric capacitor is connected between said means for connecting and said means for receiving.

7. A non-volatile memory cell, comprising:

a ferroelectric capacitor for storing first and second polarization states therein, whereby said polarization states correspond respectively to data states for storage in said memory cell,

a bit line for providing data signals to said ferroelectric capacitor and for receiving data signals from said ferroelectric capacitor,

a drive line for supplying predetermined drive pulses to said ferroelectric capacitor for setting said polarization states into said ferroelectric capacitor due to electric fields between said drive line and said bit line and said drive pulses for reading said polarization states from said ferroelectric capacitor by charge transfer to said bit line, and

an access transistor connected to said ferroelectric capacitor for selectively connecting said ferroelectric capacitor serially between said bit line and said drive line.

8. A non-volatile memory cell as recited in claim 7 wherein said access transistor is a field effect transistor having the gate terminal thereof connected to a word line to receive a selection signal for said memory cell, and having the source and drain terminals thereof connected between a terminal of said capacitor and either said drive line or said bit line.

9. A non-volatile memory cell, comprising:

a ferroelectric capacitor for storing first and second polarization states and having first and second terminals,

a drive line connected to the first terminal of said ferroelectric capacitor, said drive line for receiving drive pulses for application to said ferroelectric capacitor,

a transistor having a first terminal for receiving a memory circuit selection signal for activating said transistor to lower the impedance between second and third terminals thereof, said second transistor terminal connected to said second terminal of said ferroelectric capacitor, and

a bit line connected to the third terminal of said transistor, said bit line for transferring data signals to said transistor and receiving data signals from said transistor, said data signals corresponding respectively to the polarization states of said ferroelectric capacitor.

10. A non-volatile memory cell as recited in claim 9 wherein said transistor is an MOS transistor, said first terminal is a gate terminal of said MOS transistor, and said second and third terminals are source and drain terminals of said transistor.

11. A non-volatile memory cell as recited in claim 9 including a word line connected to supply said selection signal to said transistor, said word line positioned perpendicular to said bit line, and said drive line positioned parallel to either said bit line or said word line.

12. A non-volatile memory cell, comprising:

first and second ferroelectric capacitors for storing polarization states corresponding to data states

first and second access transistors corresponding respectively to said first and second ferroelectric capacitors,

a drive line, a first bit line and a second bit line, said first capacitor and said first transistor connected serially between said drive line and said first bit line, said second capacitor and said second transistor connected serially between said drive line and said second bit line, and

a word line connected to the control terminals of said access transistors for turning on said access transistors upon receipt of a selection signal for said memory cell to permit reading the polarization states stored in said capacitors thereby reading a data state from said memory cell or setting polarization states into said capacitors thereby storing a data state into said memory cell.

13. A non-volatile memory cell as recited in claim 12 including a differential sense amplifier having said first and second bit lines connected to the inputs thereof for differentially driving said bit lines to inverse voltage states representing a data state read from said memory cell.

14. A non-volatile memory cell as recited in claim 12 including a differential sense amplifier having the input terminals thereof connected to said first and second bit lines and further including a data input terminal for receiving a data state therethrough for driving said bit lines to differential voltage states by operation of said sense amplifier to store opposite polarization states in said ferroelectric capacitors.

15. A non-volatile memory cell as recited in claim 12 including means for equalizing the charge states on said first and second bit lines.

16. A non-volatile memory circuit, comprising:

a plurality of memory cells each comprising a ferroelectric capacitor connected in series with an access transistor between a plurality of respective drive lines and a common bit line,

a plurality of word lines connected respectively to control terminals for a plurality of said access transistors for activating respective ones of said access transistors upon receipt of a selection signal for one of said memory cells, and

a differential sense amplifier for reading from and writing to said memory cells, said sense amplifier having a first input connected to said bit line connected to said selected memory cell and a second input thereto connected to receive a reference signal, said sense amplifier having a data input/output terminal, said sense amplifier for differentially driving said first and second input lines for reading a data state from one of said memory cells connected thereto and for applying the data state thus read to said input/output terminal, and said sense amplifier for driving said bit lines connected to said selected memory cell to one of a set of predetermined voltage states corresponding to a data state received at said input/output terminal for writing said received data state into the selected one of said memory cells.

17. A non-volatile memory circuit as recited in claim 16 wherein said reference signal is a predetermined voltage.

18. A non-volatile memory circuit as recited in claim 16 including a respective complementary memory cell for each of said plurality of memory cells wherein the output of the corresponding complementary memory cell is transmitted through a bit line to provide said reference signal to said sense amplifier.

19. A non-volatile memory circuit as recited in claim 16 including multiple sets of said memory cells, each set having a respective common bit line thereby forming a memory circuit matrix comprising runs and columns of said memory cells.

20. A non-volatile memory circuit as recited in claim 16 including means for isolating said sense amplifier from said bit line.

21. A non-volatile memory cell as recited in claim 16 including a dummy ferroelectric capacitor memory cell for said plurality of memory cells and a bit line connected to provide the output of the dummy memory cell as the reference signal to said sense amplifier.

22. A non-volatile memory circuit, comprising:

a plurality of memory cells each comprising a ferroelectric capacitor connected in series with an access transistor between a plurality of respective bit lines and a common drive line,

a word line connected to control terminals for said access transistors for activating said transistors upon receipt of a selection signal for one of said memory cells, and

a plurality of differential sense amplifiers corresponding respectively to said bit lines for reading from and writing to said memory cells, each sense amplifier having a first input connected to the corresponding bit line and a second input connected to receive a reference signal, each said sense amplifier having a data input/output terminal, said sense amplifier for differentially driving said first and second inputs thereof for reading a data state from the one of said memory cells connected thereto, and for applying the data state then read to said input/output terminal, and said sense amplifiers for driving the corresponding bit lines connected to said memory cells to predetermined voltage states corresponding to a data state received at said input/output terminal for writing said received data state into the corresponding one of said memory cells.

23. A non-volatile memory circuit as recited in claim 22 wherein said reference signal is a predetermined voltage.

24. A non-volatile memory circuit as recited in claim 22 including a respective complimentary memory cell for each of said plurality of memory cells wherein the output of the corresponding complimentary memory cell for each of said plurality of memory cells wherein the output of the corresponding complimentary memory cell is transferred through a bit line to provide said reference signal to the second input of the corresponding sense amplifier.

25. A non-volatile memory circuit as recited in claim 22 including multiple sets of said memory cells, each set having a respective common drive line thereby forming a memory circuit matrix comprising rows and columns of said memory cells.

26. A non-volatile memory circuit as recited in claim 22 including respective means for isolating said sense amplifier from the coresponding bit lines.

27. A method for writing a data state into a non-volatile memory cell, comprising the steps of:

selecting said memory cell by activating an access transistor to connect a ferroelectric capacitor between a drive line and a bit line,

applying a drive pulse through said drive line to a first terminal of said ferroelectric capacitor,

applying a data signal, which has one of a plurality of voltage states, through said bit line to a second terminal of said ferroelectric capacitor wherein the voltage difference between said drive signal and said data signal establishes a given polarization state to said ferroelectric capacitor, said given polarization state corresponding to said data signal, and

deactivating said access transistor to isolate said ferroelectric capacitor after said ferroelectric capacitor has been set to said given polarization state.

28. A method for writing a data state into a non-volatile memory cell as recited in claim 27 wherein said drive pulse has first and second sequential states for respectively establishing opposite polarization states in said ferroelectric capacitor.

29. A method for writing a data state into a non-volatile memory cell as recited in claim 27 wherein the step of deactivating said access transitor occurs prior to the termination of said data signal.

30. A method for writing a data state into a non-volatile memory cell as recited in claim 27 wherein the step of deactivating said access transistor occurs after termination of said data signal.

31. A method for reading data states from a non-volatile memory cell, comprising the steps of:

selecting said memory cell by activating an access transistor to connect a ferroelectric capacitor between a drive line and a bit line,

applying a predetermined drive pulse through said drive line to a first terminal of said ferroelectric capacitor, said ferroelectric capacitor having one of a plurality of polarization states set therein,

producing a charge signal at said bit line in response to said drive pulse applied to said ferroelectric capacitor wherein the amplitude of said charge signal is a function of the polarization state stored in said ferroelectric capacitor, and

comparing said charge signal to a reference signal to produce a first data state if said charge signal is greater than said reference signal or a second data state if said charge signal is less than said reference signal.

32. A method for reading data states from a non-volatile memory as recited in claim 31 including the step of driving said bit line to such a voltage state relative to the voltage state at said drive line to produce an electric field across said ferroelectric capacitor to reestablish the original polarization state therein.

33. A method for reading data states from a non-volatile memory cell as recited in claim 31 wherein the step of comparing said charge signal to a reference signal occurs before the termination of said drive pulse.

34. A method for reading data states from a non-volatile memory cell as recited in claim 31 wherein the step of comparing said data signal to a reference signal occurs after the termination of said drive pulse.

35. A method for writing a data state into a non-volatile memory cell, comprising the steps of:

setting first and second bit lines to opposite signal states, said combination of states corresponding to one of a plurality of data states for storage in said memory cell,

selecting said memory cell by activating respective access transistors for first and second ferroelectric capacitors to connect said first capacitor between a drive line and said first bit line and to connect said second capacitor between said drive line and said second bit line, and

applying a drive signal through said drive line, said drive signal having first and second states wherein the signal difference across said first capacitor between said drive line and said first bit line when said drive line is at said first state sets a first polarization state in said first capacitor and the signal difference across said second capacitor between said drive line and said second bit line when said drive line is at said second state sets a second polarization state in said second capacitor whereby said first and second polarization states set respectively in said first and second capacitors represents one of said data states which is thereby stored in said memory cell.

36. A method for writing a data state into a non-volatile memory cell as recited in claim 35 wherein the step of setting first and second bit lines to opposite signal states is carried out by a differential sense amplifier receiving a data signal and driving said first and second bit lines to opposite signal states which correspond to said received data signal.

37. A method for writing a data state into a non-volatile memory cell as recited in claim 35 inlcuding the step of deactivating said access transistors prior to terminating the signal states set to said first and second bit lines.

38. A method for writing a data state into a non-volatile memory cell as recited in claim 35 inlcuding the steps of deactivating said access transistors after terminating the signal states set to said first and second bit lines.

39. A method for reading a data state from a non-volatile memory cell, comprising the steps of:

selecting said memory cell by activating first and second access transistors which correspond respectively to first and second ferroelectric capacitors to connect said first ferroelectric capacitor between a first bit line and a drive line and said second ferroelectric capacitor between a second bit line and said drive line,

said ferroelectric capacitors having inverse polarization states set therein to represent said data state,

applying a drive pulse through said drive line to each of said ferroelectric capacitors to produce respective charge signals on the corresponding bit lines wherein the amplitude of the charge signals at the respective bit lines are a function of the polarization state set in the corresponding ferroelectric said capacitor and

driving the one of said bit lines having the greater amplitude charge signal to a first predetermined voltage state and concurrently driving the one of said bit lines having the lesser amplitude charge signal to a second predetermined voltage state wherein the combination of said predetermined voltage states on said bit lines corresponds to said data state stored in said memory cell.

40. A method for reading a data state as recited in claim 39 wherein the difference between the voltage state on said first bit line and the voltage state at said drive line reestablishes a first ferroelectric capacitor.

41. A method for reading a data state as recited in claim 39 wherein the step of comparing starts prior to the termination of said drive pulse.

42. A method for reading a data state as recited in claim 39 wherein the step of comparing starts after the termination of said drive pulse.

43. A method for reading a data state from a non-volatile memory cell as recited in Claim 39 including the step of equalizing the charge on said first and second bit lines prior to the step of applying a drive pulse.

44. A method for reading and writing data states for a non-volatile memory cell, comprising the steps of:

reading said memory cell by:

(a) applying a selection signal to a word line for activating an access transistor to connect a ferroelectric capacitor between a drive line and a bit line,

(b) reading said memory cell by applying a drive pulse through said drive line to said ferroelectric capacitor for transferring charge from said capacitor to said bit line to produce a charge signal at said bit line, the amplitude of said transferred charge being a function of the previously set polarization state of said capacitor,

(c) comparing, by operation of a differential sense amplifier, the charge signal at said bit line with a reference signal and driving the bit line to a high voltage state when said charge signal is greater than said reference signal or driving said bit line to a low voltage state when said charge signal is less than said reference signal wherein said high and low voltage states represent respective data states which can be stored in said memory cell, and

writing to said memory cell by:

(a) applying a selection signal to said word line for activating said access transistor to connect said ferroelectric capacitor between said drive line and said bit line,

(b) applying a data state signal to said sense amplifier which in turn drives said bit line to one of said voltage states corresponding to the data signal provided to said sense amplifier, and

(c) applying a drive pulse to said drive line to establish an electric field across said capacitor to set a polarization state in said capacitor, said field having a polarity corresponding to said data state signal applied to said sense amplifier thereby storing said data state as a polarization state in said ferroelectric capacitor of said memory cell.

45. A method for reading and writing data states as recited in claim 44 wherein the step of comparing starts before the termination of said drive pulse.

46. A method for reading and writing data states as recited in claim 44 wherein the step of comparing starts after the termination of said drive pulse.

47. A method for reading and writing data states as recited in claim 44 wherein the high or low voltage state produced by said step of comparing produces an electric field across said ferroelectric capacitor relative to the drive line, to reestablish the original polarization state in said ferroelectric capacitor when that state has been destructively read.

48. A method for reading and writing data states as recited in claim 44 inlcuding the step of deactivating said selection signal prior to terminating said applied data state signal.

49. A method for reading and writing data states as recited in claim 44 including the step of deactivating said selection signal after terminating said applied data state signal.

50. A method for reading and writing data states for a non-volatile memory cell as recited in claim 44 including the step of isolating said sense amplifier from said bit line prior to the step of comparing.

51. A method for reading a non-volatile memory cell, comprising the steps of:

activating an access transistor to connect a ferroelectric capacitor serially between a bit line and a drive line, said ferroelectric capacitor having a previously set polarization state,

applying a drive pulse through said drive line to said ferroelectric capacitor for transferring predetermined charge to said bit line, the amplitude of said transferred charge being a function of the polarization state of said ferroelectric capacitor whereby a charge signal is established at said bit line, wherein the amplitude of said charge signal is related to the amplitude of said charge transfer,

comparing said charge signal at said bit line with a reference signal and differentially driving said bit line to either a high or low voltage state as determined by the difference between said charge signal and said reference signal, and

restoring said previously set polarization state to said ferroelectric capacitor by action of the electric field between said bit line and said drive line thereby reestablishing the original data state in said memory cell.

52. A method for reading a non-volatile memory cell as recited in claim 51 wherein the step of comparing starts before the termination of said drive pulse.

53. A method for reading a non-volatile memory cell as recited in claim 51 wherein the step of comparing starts after the termination of said drive pulse.

54. A method for writing a data state into a non-volatile memory cell, comprising the steps of:

applying a selection signal to first and second access transistors for respectively connecting a first ferroelectric capacitor between a drive line and a first bit line and a second ferroelectric capacitor between said drive line and a second bit line,

applying one of a set of differential voltage states to said bit lines in which each of said differential voltage states corresponds to a data state, and

applying a drive signal having sequentially a first voltage state and a second voltage state whereby the voltage difference between said first voltage state at said drive line and the voltage state at said first bit line establishes a first polarization state in said first ferroelectric capacitor and the voltage difference between said second voltage state and said second bit line establishes a second polarization state in said second ferroelectric capacitor wherein the combination of said first and second polarization states stored in said first and second ferroelectric capacitors corresponds to said data state.

55. A method for writing a data state into a non-volatile memory cell as recited in claim 54 wherein the step of applying one of a set of differential voltage states is carried by a differential sense amplifier which receives a data state and drives said bit lines to one of said differential voltage states corresponding to said data state.

56. A method for writing a data state into a non-volatile memory cell as recited in claim 54 including the step of deactivating said selection signal prior to terminating said differential voltage states applied to said bit lines.

57. A method for writing a data state into a non-volatile memory cell as recited in claim 54 including the step of deactivating said selection signal after terminating said differential voltage states applied to said bit lines.

58. A read/modify/write cycle for a non-volatile memory cell, comprising the steps of:

activating an access transistor to connect a ferroelectric capacitor between a drive line and a bit line wherein said ferroelectric capacitor stores polarization states which correspond to respective data states,

applying a first drive pulse through said drive line to said ferroelectric capacitor to transfer a variable amount of charge to said bit line depending on the polarization state of said ferroelectric capacitor,

comparing the voltage on said bit line due to said transferred charge to a reference voltage by operation of a sense amplifier and during said bit line to a first state when the bit line voltage exceeds the reference voltage and to a second state when the bit line voltage is less than the reference voltage,

transferring said first or second state from said bit line to an input/output line while said access transistors are activated,

applying a data state to said input/output line while said access transistors are activated,

transferring said data state from said input/output terminal to said bit line,

applying a second drive pulse through said drive line to produce an electric field across said ferroelectric capacitor between said drive line and said bit line to set a polarization state into said ferroelectric capacitor, said polarization state corresponding to said data state applied to said input/output terminal, and

deactivating said access transistor to isolate said ferroelectric capacitor.

59. A read/modify//write cycle for a non-volatile memory cell as recited in claim 58 including the step of isolating said bit line from said sense amplifier during said step of comparing and driving.

60. A read/modify/write cycle for a non-volatile memory cell as recited in claim 58 including the step of comparing comprises comparing the voltage on a second bit line connected to a complimentary ferroelectric capacitor which has stored therein an opposite polarization state from that of said first ferroelectric capacitor.

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